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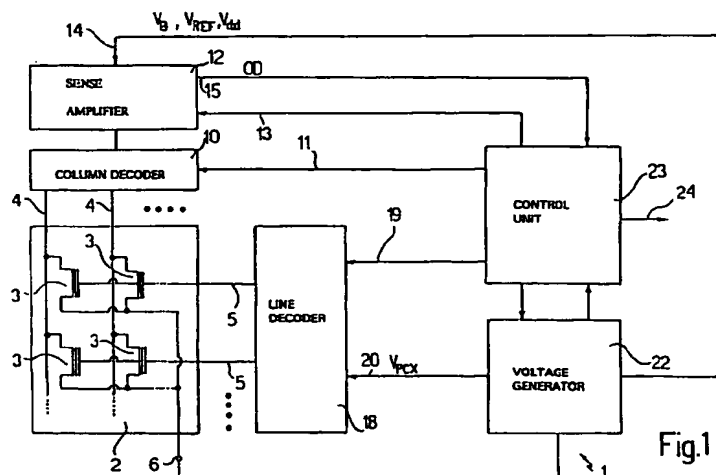
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(54) Method for controlled erasing memory devices, in particular analog and multi-level flash-EEPROM devices

(57) The controlled erase method includes supplying (40) at least one erase pulse to cells (3) of a memory array (2); comparing (53) the threshold voltage of the erased cells with a low threshold value; selectively soft-programming (62) the erased cells which have a threshold voltage lower than the low threshold value; and verifying (42) whether the erased cells have a threshold voltage lower than a high threshold value, which is

higher than the low threshold value. If at least one pre-determined number of erased cells has a threshold voltage which is higher than the high threshold value, an erase pulse is applied (44) to all the cells and the steps of comparing, selectively soft-programming and verifying are repeated.



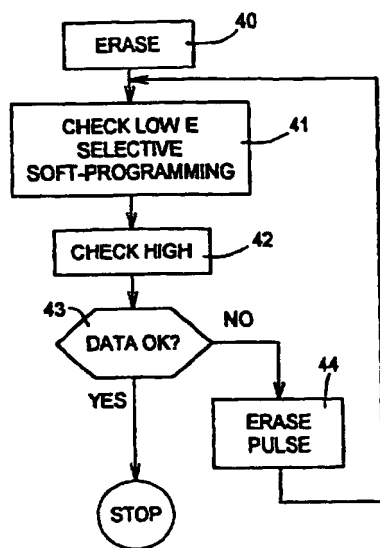


FIG. 3

Description

[0001] The present invention relates to a method for controlled erasing non-volatile memory devices, in particular analog and multi-level flash-EEPROM devices.

[0002] As is known, two main problems are encountered when flash cells are erased, after application of one or more erase pulses, i.e. some of the cells are erased excessively, so that they have a negative threshold voltage (depleted cells); and after a long erase pulse the dispersion of the threshold voltages is large (up to approximately 3 V).

[0003] Furthermore, after erasing, in order to permit subsequently correct data storage, in particular if the memory is of the analog or multi-level type and storage of different digital values or analog values is involved, no depleted cells should be present, and the cells cannot have a threshold voltage which is lower than a specific value. The aforementioned requirements cannot be met when, in addition to cells which behave correctly, there are cells which, at each erase pulse, modify their threshold voltage too little, as well as cells which modify their threshold voltage excessively.

[0004] At present, erasing is carried out such that its duration is minimised, without imposing excessively narrow constraints on the final distribution of the threshold voltage. For this purpose, erasing is generally carried out by supplying erase pulses of a predetermined duration (for example 10 ms), each followed by an erase verify step on a subassembly of cells (which normally all belong to a whole row of the sector which is being erased). If at least one cell of the subassembly does not pass the verify step (since it has a threshold which is higher than a predetermined value), a new erase pulse is supplied. When all the cells of the subassembly pass the verify step, the entire sector is verified until a percentage near 100% (e.g. 98%) passes the verifying step. At the end of erasing, in order to recover depleted cells, a soft-programming pulse is generated (i.e. by supplying a gate voltage of $V_G = 7$ V, and a drain voltage of $V_D = 7$ V for a period of approximately 5 μ s), blindly to all the cells.

[0005] However the above-described erase method cannot provide the requirements of dispersion amplitude and low average value necessary for analog or multi-level programming.

[0006] The object of the invention is thus to provide an erase method which makes it possible to obtain the aforementioned requirements.

[0007] According to the present invention, there is provided a method for controlled erasing non-volatile memory devices, in particular analog and multi-level flash-EEPROM devices, as defined in claim 1.

[0008] To assist understanding of the present invention, a preferred embodiment is now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- figure 1 shows a simplified block diagram of a flash memory of a known type;
- figure 2 shows a circuit diagram of a block of figure 1; and
- figures 3-5 are flowcharts relative to the present method.

[0009] Figure 1 shows the blocks of a memory 1, which intervene during erasing. In detail, of the memory 1, there is shown an array 2 comprising a plurality of cells 3 arranged on rows and columns and connected to respective bit lines 4 and word lines 5; in detail, and in known manner, the cells 3 which are disposed on a single column have drain terminals connected to a single bit line 4; the cells 3 which are disposed on a single row have gate terminals connected to a single word line 5, and all the source terminals are connected to one another and are available outside the array 2 through a common source terminal 6. In a known manner, if the array 2 were divided into sectors, the common source terminals 6 would be separated for the various sectors.

[0010] The bit lines 4 are connected to a column decoder 10, which, as specified by address signals supplied to a control input 11 of the decoder, connects the bit lines 5 selectively in a known manner to a bias and read circuit (sense amplifier 12), which is shown in greater detail in figure 2. Sense amplifier 12 has a control input 13, a bias input 14 receiving voltages V_B and V_{REF} as well as the supply voltage V_{dd} and an output 15, to which output data OD are supplied. Similarly, word lines 5 are connected to a row decoder 18 having a control input 19 which receives address signals, and a bias input 20 which receives a voltage V_{PCX} .

[0011] Bias and supply voltages V_B , V_{REF} , V_{dd} and V_{PCX} are generated by a generator stage 22 connected to the common source terminal 6, which is controlled by a control unit 23, and in turn supplies the control unit 23. The latter (which comprises e.g. a state machine) supplies address signals to column decoders 10 and row decoders 18, receives output signal OD from sense amplifier 12, and has an output 24 for connection to the other parts (not shown) of memory 1.

[0012] The structure of sense amplifier 12 is shown in detail in figure 2, and is described here briefly only, since it is of a conventional type. In figure 2, of the array 2, there is shown a single cell 3, connected to a first node 28 of a current mirror circuit 29 via a switch 27 belonging to column decoder 10 and to a cell bias circuit 30. Cell bias circuit 30 is connected to a control transistor 31 of PMOS type, which has a gate terminal connected to input 13 and a source terminal connected to input 14, and receives voltage V_B , which, neglecting the voltage drop on control transistor 31, is applied to the drain terminal of cell 3, as planned in the various reading and writing steps of cell 3.

[0013] Current mirror circuit 29 has a second node 32 connected via a reference bias circuit 33 to a reference transistor 34 of NMOS type, which has a source termi-

nal connected to ground and a gate terminal connected to input 14 of sense amplifier 12, and which receives voltage V_{REF} . Reference bias circuit 33 has the same structure as cell bias circuit 30, but is not connected to any control transistor.

[0014] Nodes 28 and 31 of current mirror circuit are connected respectively to a first and a second input node 35 and 36 of a single-ended differential circuit 37 of MOS type, per se known and not described further, the output node 38 of which is connected to output terminal 15 of sense amplifier 12 via an inverter 39.

[0015] In a known manner, when appropriate voltage values V_{PCX} and V_{REF} are supplied to word line 5 of connected cell 3, and to the input 14, sense amplifier 12 compares the currents flowing in cell 3 and in reference transistor 33 and generates a first logic state (in this case a "1") of signal OD, if the threshold voltage of cell 3 is lower than a value which is correlated to voltage V_{REF} and vice versa. In addition, since comparison is made in current, the greater is the voltage value compared to the threshold voltage of cell 3, the smaller is the reference voltage V_{REF} supplied to reference transistor 33.

[0016] On this basis, the method for controlled erasing array 2 is now described with reference to figure 3 and to circuit diagrams of figures 1 and 2. Initially, block 40, a first programming pulse is applied. For this purpose, for a predetermined period of, for example 10 ms, a voltage of 10 V is supplied to common source terminal 6, voltage V_{PCX} of all word lines 5 is set to ground (0 V), and all bit lines 4 are left floating (by opening all switches 27 of column decoder 10).

[0017] Then, block 41, a low threshold verify step ("check low") is carried out on all cells of the array (or of the erased sector); if one or more cells 3 is over-erased, i.e. if its threshold is lower than a first threshold value V_{th1} , selective "soft" programming is carried out only of the over-erased cell or cells, as described in detail hereinafter with reference to figure 4.

[0018] Subsequently, block 42, a high threshold verify step ("check high") is carried out; if all cells have a threshold voltage lower than a second threshold value V_{th2} but greater than the first (YES output from block 43), the erase process is terminated; in the opposite case (NO output), a further erase pulse is supplied (block 44) and the described process is repeated from beginning.

[0019] With reference to figure 4, the low threshold verify step is now described in detail. In particular, this step takes into account that incorrect reading of an addressed cell can be caused not by the addressed cell itself, but by another depleted cell in the same column, which conducts even if it is not addressed (with a zero gate voltage); consequently if there is a depleted cell in a column, it is not always possible to locate this cell accurately immediately. In this case, as described hereinafter in detail, the cell which gives rise to incorrect reading receives a series of soft programming pulses

and is read once more after each soft pulse; if at a given moment this cell generates a correct reading, low threshold of the next cell takes place; on the other hand if, after a predetermined number of pulses and corresponding verify steps, the cell still appears to be over-erased, the process continues by verifying the successive cells, and the anomaly encountered is stored by a flag. After verifying all cells of the memory (or of the erased sector), if the flag indicates the described abnormal situation, an entire low threshold verify process is repeated once more on the entire memory, using the same methods previously described. Thereby, in general it is possible to correct an over-erase condition, even if the over-erased cell is not located correctly within a column.

[0020] Therefore, with reference to figure 4, reference voltage V_{REF} applied to reference transistor 33 in figure 2 is set for example to 2.5 V, voltage V_{PCX} supplied to row decoder 18 is set to 3 V, and voltage V_B is set to 5 V, block 50. Then, a cell counter I (used to address each time a single cell to be verified) and the flag, indicated SW, are initialised to zero, block 51. Output signal OD is then read by sense amplifier 12 (block 52); as explained earlier with reference to figure 2, if threshold voltage of read cell 3 is lower than first predetermined value V_{th1} correlated to voltage V_{REF} (cell 3 conducting), the output signal is equal to 0, and in the opposite condition it is equal to 1. It is then checked whether OD is equal to 0, block 53; if this is the case (YES output), counter I is incremented for verifying a successive cell, block 54. It is then checked whether the entire memory has not already been verified (block 55); if not, the program returns to block 52 for reading a successive cell; if the entire memory has been verified, it is checked whether flag SW is equal to 0. If this is the case (low threshold verify correct for all the cells of the memory), the process ends; if this is not the case, the program returns to block 51 for repetition of the low threshold verify step on the entire memory (or memory sector).

[0021] If, during verify of a cell 3, the latter is found to be over-erased, and thus output signal OD is equal to 1 (NO output from block 53), soft-programming of the over-erased cell is carried out. In detail, block 60, a repetition counter C is initially set to zero; repetition counter C is then incremented by one unit (block 61); voltage V_{PCX} (applied to the word line which is connected to the cell to be soft-programmed) is set to 5 V for a predetermined time t_1 (eg 1 μ s), block 62, whereas drain voltage V_D remains at approximately 5 V, such that a programming pulse is applied to the depleted cell 3. Voltage V_{PCX} is then set once more to the reading value of 3 V, block 63, and the threshold voltage of just soft-programmed cell 3 is read (block 64). The value of output signal OD is then checked (block 65); if this is equal to 0, i.e. if the just soft-programmed cell is no longer in the over-erased condition, the process continues with verifying a successive cell, with return to block 54; if this is not the case, it is checked whether a predetermined

number of soft-programming pulses, for example 10, has already been supplied, block 66. If not, there is a return to block 61, counter C is incremented, and a further soft-programming pulse is supplied to depleted cell 3; if yes, anomaly flag SW is set to 1, block 67, and verify continues with successive cells.

[0022] The high threshold verify process is now described with reference to figure 5. Initially, voltage V_{REF} is set to 2 V, and voltage V_{PCX} is set to 3 V (which, as already explained, corresponds to comparing threshold voltage of cells 3 with second threshold value V_{th2} , which is greater than V_{th1}), block 70. Cell counter I is then initialised to zero, block 71, and verify reading of the first cell is carried out, acquiring the logic value of output signal OD, block 72. It is then checked whether this logic value is equal to 1 (corresponding to the situation in which cell 3 is conducting, i.e. when it has a threshold voltage which is lower than the second value), block 73; if this is not the case, an incorrect datum indicator is set, block 77, and the high threshold verify process terminates; if the result is positive, counter I is incremented, block 74, in order to address a successive cell, and it is checked whether the entire memory has been examined, block 75. If further cells 3 of the memory need to be verified, NO output from block 75, there is a return to reading block 72 of output signal OD for the successive cell; otherwise, YES output, a correct datum indicator is set, block 76, and the high threshold verify process ends.

[0023] The described erase method has the advantage that it provides for a close distribution of threshold voltages of the erased cells (and more specifically, it is possible to set the distribution amplitude by appropriate selection of voltage values V_{REF} during the low and high threshold verify steps), as well as the average value of the threshold voltages. The erase method can be carried out by circuitry and steps already present in the memory, without requiring structural modifications of the latter, on the basis of a programme stored in control unit 23.

[0024] Finally, it is apparent that numerous changes and variants can be made to the described and illustrated method, all of which come within the scope of the inventive concept, as defined in the attached claims. For example, instead of measuring a single cell which is not sufficiently erased, as described above, a new programming pulse and repetition of the low and high threshold verify steps can be applied only if the cells which are not sufficiently erased are greater than a specific number, or in the case of a large difference between the high threshold voltage to be compared and the threshold voltage of the insufficiently erased cell, if the memory includes circuitry which makes it possible to detect this difference. In addition, it is possible to carry out high threshold and low threshold verify reading, and to supply the soft-programming pulses in parallel to several cells (e.g. eight or sixteen cells connected to the same word line 5), by providing appropriate parallel reading

circuits (similarly to the process normally used at present for reading the cells), as well as circuits for selecting the cells, from those read simultaneously, which require soft programming pulses.

Claims

1. A method for controlled erasing non-volatile memory devices, in particular flash-EEPROM devices, comprising the steps of supplying (40) at least one erase pulse to cells (3) of a memory array (2) and verifying (43) that the erased cells have a threshold voltage which is lower than a first threshold value; characterised in that it comprises the steps of:
 - comparing (53) said threshold voltage of the erased cells with a second threshold value, which is lower than said first threshold value; and
 - selectively soft-programming (62) the erased cells which have a threshold voltage lower than said second threshold value.
2. A method according to claim 1, characterised in that said steps of comparing (53) and selectively soft-programming (62) are carried out before said step of verifying (43).
3. A method according to claim 2, characterised in that after said step of verifying (43), if at least one pre-determined number of erased cells has a threshold voltage which is higher than said first threshold value, the step is carried out of applying (44) an erase pulse to said erased cells and repeating said steps of comparing, selectively soft-programming and verifying.
4. A method according to any of the preceding claims, characterised in that said step of comparing comprises the steps of:
 - a) addressing (51) a first cell from said erased cells;
 - b) read biasing said cell addressed;
 - c) generating (52) a first comparison signal (OD) which has a first comparison value, if said addressed cell (3) has a threshold voltage which is greater than said second threshold value, and otherwise generating a second comparison value;
 - d) if said first comparison signal (OD) has said first comparison value, addressing (54) a cell following said addressed cell, from said erased cells, and returning to said step b);
 - e) if said first comparison signal (OD) has said second comparison value, updating (61) a repetition counter (C); applying (62) a soft-programming pulse to said addressed cell; read

biasing (63) said addressed cell; and updating (64) said first comparison signal;

f) if said first comparison signal (OD) has said first comparison value, addressing (54) a cell (3) following said addressed cell, and returning to said step b);

g) if said first comparison signal has said second comparison value, and said repetition counter (C) is lower than a predetermined repetition value, returning to said step e);

h) if said first comparison signal has said second comparison value, and said repetition counter (C) is higher than a predetermined repetition value, addressing (54) a cell following said addressed cell and returning to said step b).

5. A method according to claim 4, characterised in that, in said step h) an anomaly signal (SW) is generated; and in that on completion of said steps of comparing (53) all said cells erased, in the presence of said anomaly signal (SW), said steps from a) to h) are repeated.

6. A method according to any one of the preceding claims, characterised in that said step of verifying (42) comprises the steps of:

i) addressing (71) a first cell from said erased cells;

j) read biasing (70) said addressed cell;

k) generating (72) a second comparison signal (OD) having a third comparison value, if said cell addressed (3) has a threshold voltage which is lower than said first threshold value, and otherwise a fourth comparison value;

l) if said second comparison signal (OD) has said third comparison value, addressing (74) a cell following said addressed cell and returning to said step j); and

e) if said second comparison signal has said fourth comparison value, generating (77) an incorrect erase signal; applying (44) an erase pulse to said cells, and repeating said steps of comparing and selectively verifying.

7. A non-volatile memory device (1), in particular a flash-EEPROM device, comprising a memory array (2) comprising a plurality of cells (3); address circuits (10, 18), connected to said memory array, for addressing one of said cells; a read and comparison circuit (12), connected to said memory array through said address circuits; an operative voltage generation unit (22) connected to said address circuits (10, 18), to said memory array (2), and to said read and comparison circuit (12); and a control unit (23), connected to said address circuits, to said read and comparison circuit and to said operative

voltage generation unit; said control unit (23) comprising erase pulse generation control means (40, 44), connected to said address circuits and to said operative voltage generation unit, and controlling transmission of an erase pulse to said cells, and verify means (43) connected to said read and verify circuit and verifying whether the erased cells have a threshold voltage lower than a first threshold value; characterised in that said control unit (23) comprises comparison enabling means (50-53) connected to said read and comparison circuit and to said operative voltage generation unit, and enabling comparison between the threshold voltage of the erased cells and a second threshold value lower than said first threshold value; and selective soft-programming control means (62) for selective soft-programming the erased cells which have a threshold voltage lower than said second threshold value.

8. A memory device according to claim 7, characterised in that said control unit (23) comprises detection means (43) for non-erased cells (3), detecting the presence of a predetermined number of erased cells which have a threshold voltage higher than said first threshold value; and sequential activation means enabled by said detection means (43) for not erased cells, and sequentially enabling said erase pulse generation control means (44), said comparison enabling means (50-53), said selective soft-programming control means (62), and said verify means (43).

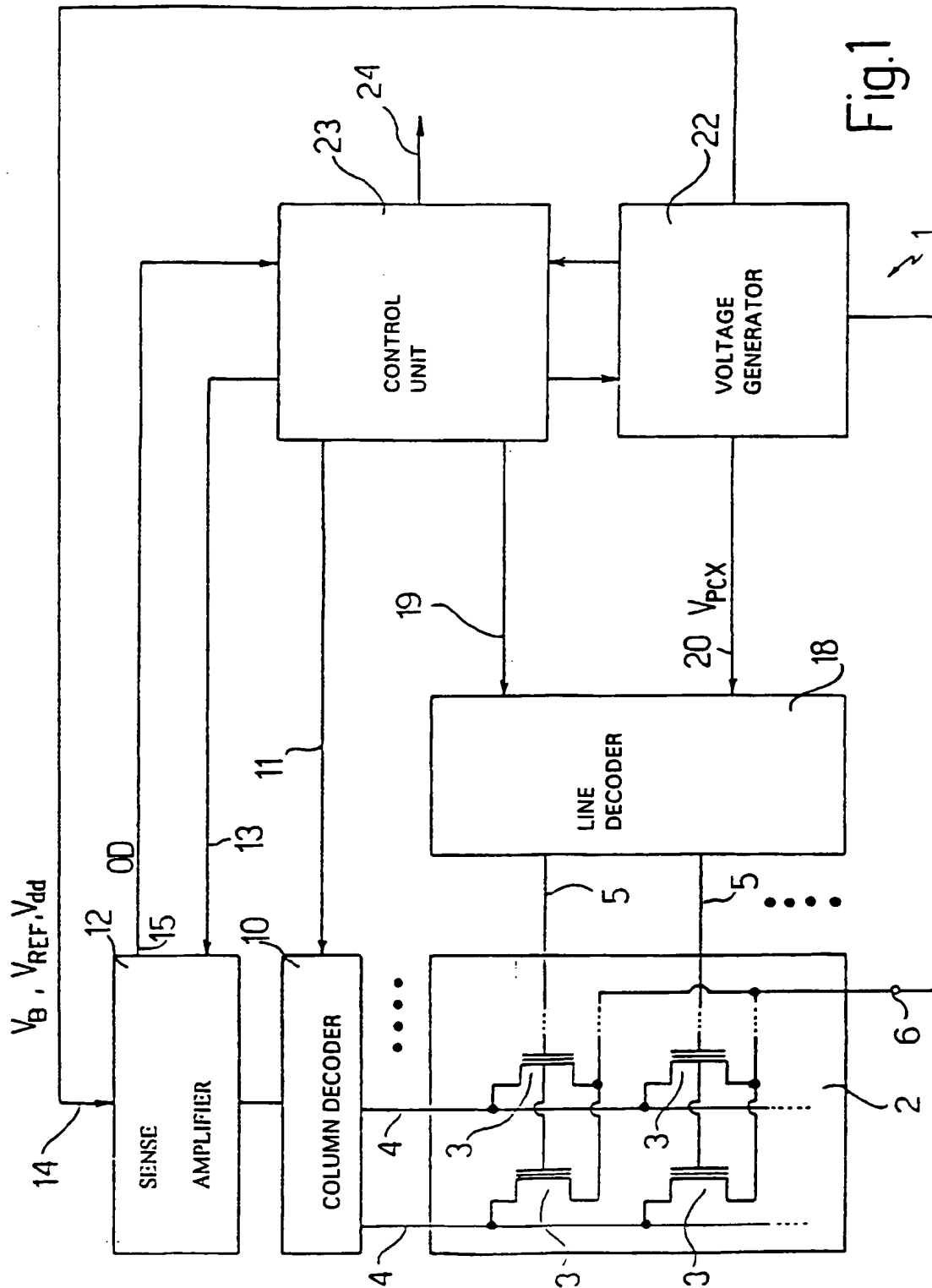


Fig. 1

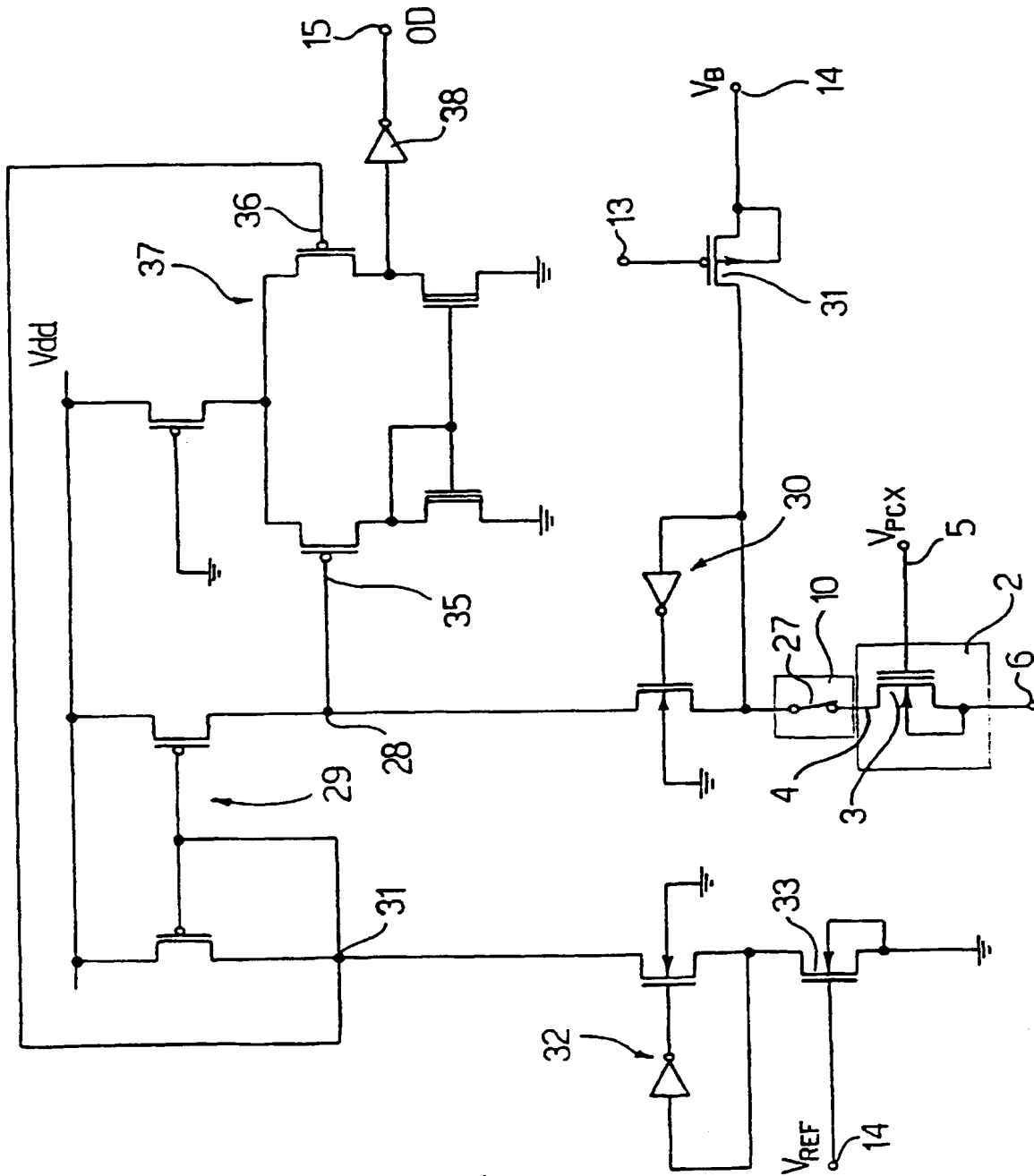


Fig.2

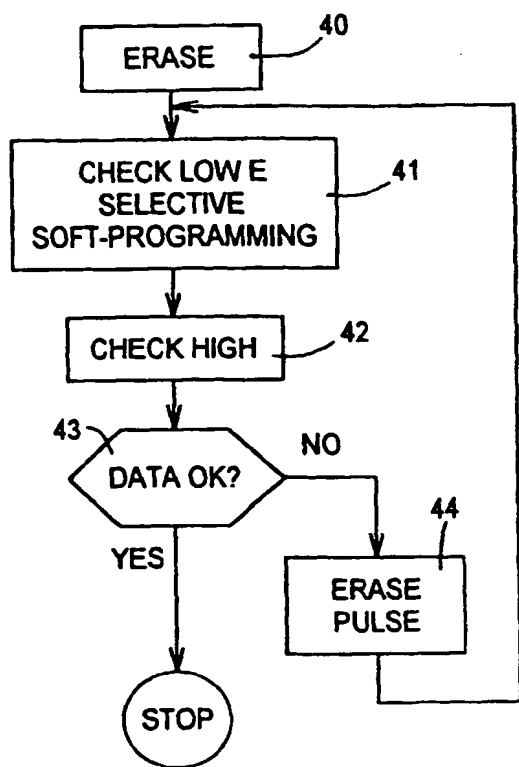


FIG. 3

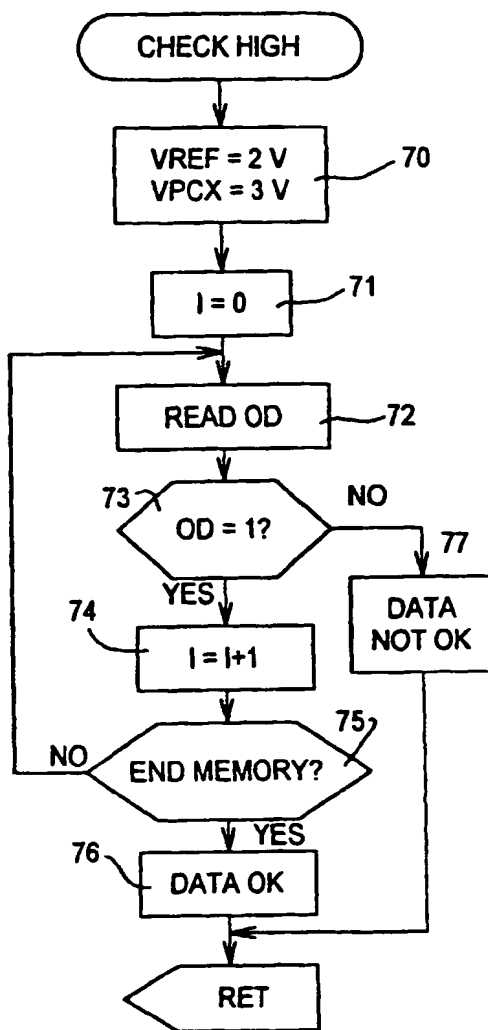


FIG. 5

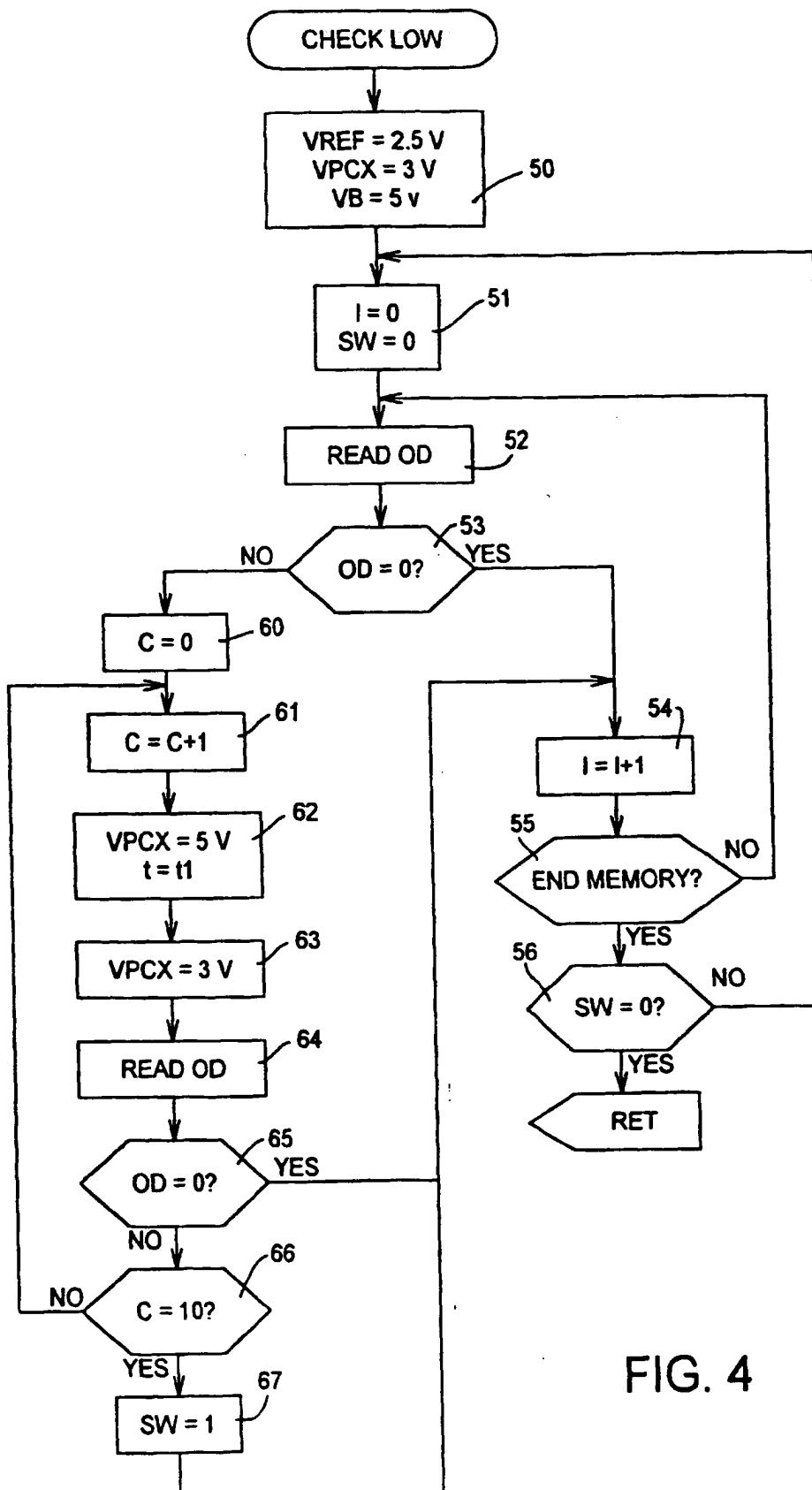


FIG. 4



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Application Number
EP 98 83 0024

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 5 636 162 A (COFFMAN TIM M ET AL) 3 June 1997	1-3,6-8	G11C16/00 G11C16/06
A	* the whole document *	4,5	
Y	EP 0 704 853 A (NIPPON ELECTRIC CO) 3 April 1996 * column 4, line 33 - column 6, line 15 * * column 8, line 17 - column 10, line 37; figure 9 *	1-3,6-8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G11C
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		18 June 1998	Czarik, D
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